Current Saturation in Submicrometer Graphene Transistors with Thin Gate Dielectric: Experiment, Simulation, and Theory

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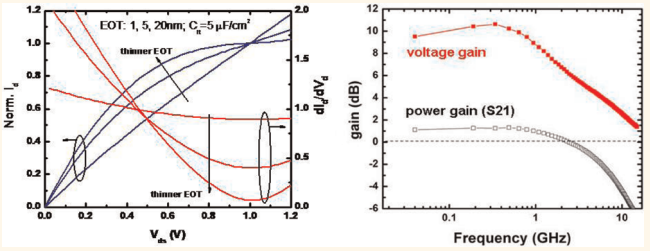
ABSTRACT



Recently, graphene field-effect transistors (FET) with cutoff frequencies (f_T) between 100 and 300 GHz have been reported; however, the devices showed very weak drain current saturation, leading to an undesirably high output conductance (g_{ds}= dI_{ds}/dV_{ds}). A crucial figure-of-merit for analog/RF transistors is the intrinsic voltage gain (g_m/g_{ds}) which requires both high g_m (primary component of f_T) and low g_{ds}. Obtaining current saturation has become one of the key challenges in graphene device design. In this work, we study theoretically the influence of the dielectric thickness on the output characteristics of graphene FETs by using a surface-potential-based device model. We also experimentally demonstrate that by employing a very thin gate dielectric (equivalent oxide thickness less than 2 nm), full drain current saturation can be obtained for large-scale chemical vapor deposition graphene FETs with short channels. In addition to showing intrinsic voltage gain (as high as 34) that is comparable to commercial semiconductor FETs with bandgaps, we also demonstrate high frequency AC voltage gain and S21 power gain from s-parameter measurements.

KEYWORDS: graphene FET · current saturation · voltage gain · compact model

Impressively high current density and carrier mobility[1−4] exhibited by graphene make it a potential candidate for the future channel material in RF devices.[5,6] However, to interest the analog/RF community in graphene FETs, current saturation, as well as high frequency gain, must be obtained from submicrometer channel devices, especially with devices using large-scale graphene, which are more relevant for a real technology. The challenge of obtaining current saturation in graphene arises from its gapless band structure. A weak saturation-like output characteristic (or "kink") has been observed frequently in graphene transistors.[5−7] This is mainly due to the ambipolar nature of graphene. At certain drain bias, the charge neutrality point moves into the channel, and the drain current shows a saturation-like behavior. Further increase of the drain bias makes the conduction type near the drain-end change from n-type (p-type) to p-type (n-type), and the drain current shows a second linear region. It is typically undesirable to introduce this "kink" since only very weak saturation was obtained by this means in most graphene FETs. The few reports of graphene FETs that show saturated output characteristics based on phonon scattering (velocity saturation) consist of devices fabricated from mechanically exfoliated graphene with either micrometer scale channel lengths[7−9] or an underlying high quality h-BN flake as the gate dielectric.[10] A recent report shows that current saturation from exfoliated graphene can also be observed by using a specialized pulsed $I-V$ measurement technique;[11] however, standard DC measurements of the devices yielded nonsaturating behavior along with degrading device performance at submicrometer channel lengths. The reports show current saturation in devices fabricated with large-scale CVD or SiC graphene films only for devices with several micrometer channel length.[12,13]

In this letter, we show that thinning the gate dielectric leads to strong current saturation in graphene FETs. Owing to this saturation and very high g_m from a thin gate dielectric, these devices feature both high

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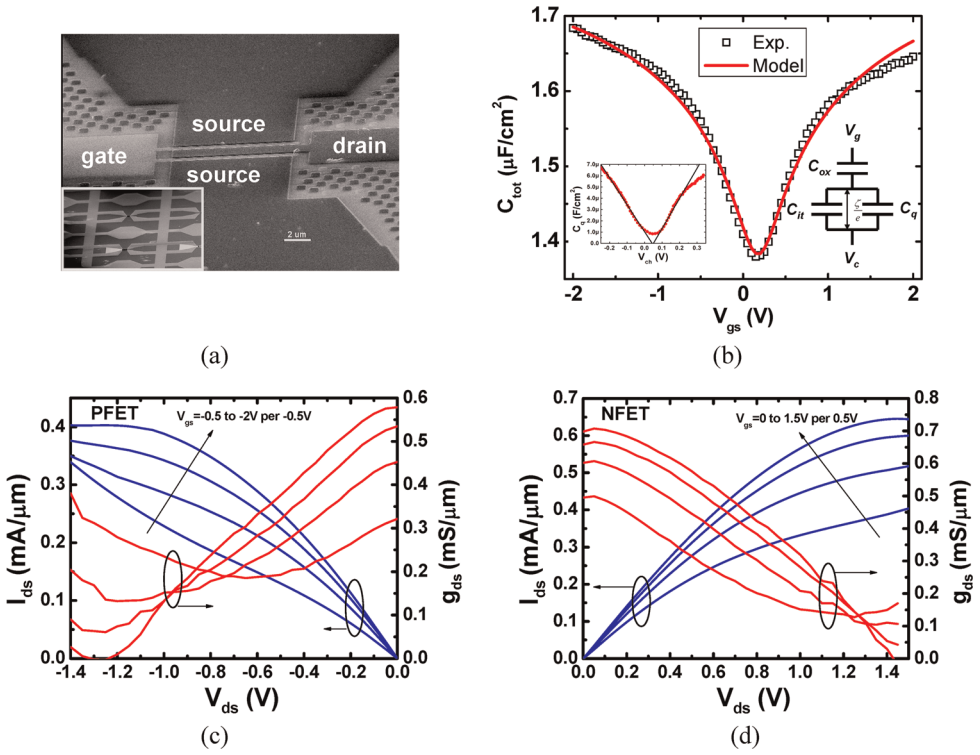

Figure 1. (a) SEM image of fabricated devices. (b) Total capacitance as a function of gate voltage. Quantum capacitance shows clear impact on the device C_{tot} due to the thin EOT. The inset shows extracted C_q as a function of the graphene channel potential (V_{ch}). (c) Output $I_{ds}-V_{ds}$ for PFET operation at different V_{gs}. (d) $I_{ds}-V_{ds}$ for NFET operation. Both PFET and NFET show clear drain current saturation.

DC voltage gain (as high as 34) that is comparable to semiconductor FETs with bandgaps[14,15] and AC voltage gain (up to 11 dB) when driving an infinite load impedance. More importantly, they also have power gain when driving a 50 ohm load impedance. We investigate the mechanisms of the observed current saturation with the derived model. It is shown that graphene's low density state (DOS) plays an important role in obtaining the saturated characteristics in thin dielectric devices. In addition, the improved electrostatic control in these devices reduces the effect of the interface trap capacitance and helps maintain the saturation behavior when a high density of traps exists. This work presents a new path to achieving current saturation in graphene FETs with gapless channels.

RESULTS AND DISCUSSION

One of the performance bottlenecks in graphene devices arises from the difficulty of depositing a thin gate dielectric on the sp^2 bonded, inert carbon surface. To overcome this drawback, we utilize the unique capability of CVD-grown graphene to be transferred onto almost any substrate and developed an embedded gate device structure.[16] With the embedded gate completed, large area CVD-grown graphene film is transferred to cover the substrate. Because the gate structure is formed first on the wafer, the step of depositing a gate dielectric on graphene is eliminated and any state-of-art dielectrics can be easily employed (*e.g.*, ≈4 nm HfO_2 in our devices). The method we used to prepare monolayers of graphene is similar to ref 17. Figure 1a shows the SEM image of a fabricated device. To extract the equivalent oxide thickness (EOT) of the devices, the total capacitance (C_{tot}) was measured *versus* V_{gs} at low frequency (100 kHz), as shown in Figure 1b. C_{tot} shows a strong dependence on V_{gs} because the quantum capacitance (C_q) of graphene starts to dominate C_{tot} for thin EOT[18,19]—the geometric gate capacitance and quantum capacitance are series components of C_{tot}. Following a previously reported method,[19] with $C_{ox} \approx 1.98\ \mu F/cm^2$ and $C_{it} \approx 3.7\ \mu F/cm^2$ (interface trap capacitance), C_q is obtained as an expected linear function of the potential of graphene (Figure 1b inset, $V_{ch} = \zeta/e = V_g C_{ox}/(C_{ox} + C_q + C_{it})$, $V_c = 0$). Nonzero C_q at the gate voltage corresponding to the charge neutrality point (V_{dirac}) is consistent with previous reports and is explained by electron−hole puddles that result from charged impurities. Extracted EOT from this fitted C_{ox} is ~1.75 nm, which is close to the thinnest reported for a graphene FET.[20]

Output characteristics from a PFET and an NFET with 500 nm channel lengths at various V_{gs} are shown in Figure 1c and Figure 1d, respectively. Note that both PFET and NFET operations shown here were performed with one single device by applying different bias conditions. From these output characteristics, g_{ds} was calculated and is also plotted in Figure 1c and Figure 1d.

The drain current saturation can be clearly seen at relatively low V_{ds} (<1.5 V) from both polarity devices. Under certain bias conditions (*e.g.*, $V_{gs} = -2.5$ V and $V_{ds} \approx -1.3$ V) the devices can reach full saturation (*i.e.*, $g_{ds} = 0$). Another key observation is that the g_{ds} curves show local minimum points, which occur at high source-drain fields when the device is biased at high V_{gs}. This is consistent with the above-mentioned "kink" effect where the conduction of the channel switches from n (p) type to p (n) type. Additionally, while higher V_{gs} gives rise to a larger initial g_{ds} at $V_{ds} = 0$, it yields a lower minimum g_{ds} (better saturation) which can be better seen in the PFET.

A surface potential based model for graphene FETs in the diffusive transport limit is derived and is used to investigate the much improved output characteristics from these devices. Using the equivalent capacitance circuit shown in Figure 1b, we can write the charge voltage relation for a metal−insulator−graphene structure as

$$C_{ox}\left(V_g - V_c - V_{dirac} - \frac{\zeta}{e}\right) = C_{it}\frac{\zeta}{e} - Q_g(\zeta) \quad (1)$$

where C_{ox} is the dielectric capacitance, $Q_g(\zeta) = en_i(F_1(\zeta/(k_BT)) - F_1(-\zeta/(k_BT)))$ is the charge in the graphene where F_1 is the Fermi integral of order 1, and n_i is the intrinsic carrier density at temperature T ($n_i = 9.81 \times 10^{10}$ cm^{-2} at room temperature). Assuming a constant interface trap density D_{it}, the interface trap capacitance is given by $C_{it} = e^2D_{it}$. The term on the left-hand side of eq 1 is the charge on the metal gate. The first term on the right-hand side of eq 1 is the net trapped charge and the second term is the net charge available for conduction. By scaling the variables in eq 1, we can write it in dimensionless form as

$$x = z(1 + C_1) - C_0(F_1(z) - F_1(-z)) \quad (2)$$

where $x = (V_g - V_c - V_{dirac})$, $z = \zeta/(k_BT)$, $C_1 = C_{it}/C_{ox}$, $C_0 = en_i/(C_{ox}V_{th})$, and $V_{th} = k_BT/e$. To verify the $C-V$ model, we have fit the model to the measured data, as shown in Figure 1b. The extracted dielectric capacitance agrees well with the dielectric capacitance expected from the physical thickness and from C_q-V_{ch} fitting. Also, the estimated C_{it} is about 4 μF/cm^2 which is consistent with our hardware data.

Current in graphene in the diffusive transport regime can be modeled using the drift-diffusion equation. Because graphene is degenerate, the ratio of the mobility to the diffusion constant is carrier density dependent. The total current density taking into account both the drift and diffusion terms can be written as[21]

$$J = J_n + J_P = \mu_n n\nabla U + \mu_p p\nabla U \quad (3)$$

where μ_n and μ_p represent the electron mobility and the hole mobility, respectively. We can write the electron density (n) and hole density (p) using 2 and the identity $F_1(z) + F_1(-z) = z^2/2 + 2F_1(0)$ as

$$\begin{aligned} n/n_i &= \frac{z^2}{4} + F_1(0) + \frac{x - z(1 + C_1)}{2C_0} \\ p/n_i &= \frac{z^2}{4} + F_1(0) - \frac{x - z(1 + C_1)}{2C_0} \end{aligned} \quad (4)$$

The electrochemical potential is expressed as $U = U_{eq} - eV_c$, where U_{eq} is an equilibrium chemical potential in the channel. We can now integrate eq 3 using $dU = -edV_c$ to obtain the drain to source current as

$$I_{ds} = \frac{W}{L}en_iV_{th}(\mu_{on}g(x_s, x_d, 1) + \mu_{op}g(x_s, x_d, -1)) \quad (5)$$

for a graphene FET of width W and length L. The function g is defined as

$$g(x_s, x_d, s) = \int_{x_s}^{x_d}\frac{z^2}{4} + F_1(0)\,dx + s\int_{x_s}^{x_d}\frac{x - z(1 + C_1)}{2C_0}\,dx \quad (6)$$

We can see that eq 5 is simply the result of the Pao−Sah modeling approach[21] applied to graphene. However, there is no double integral in this case because the channel is confined to a single atomic plane of the graphene. The high field mobility model is assumed to be of the form given below:

$$\mu_{n/p} = \frac{\mu_{0n/p}}{1 + \frac{\mu_{0n/p}|E|}{v_{sat}}} \quad (7)$$

where $\mu_{on/p}$ is the low field mobility for electrons/holes. Note that in the current model the low field mobility in the denominator is assumed to be same for both holes and electrons to simplify the equations. Saturation velocity in graphene is modeled as $v_{sat} = \hbar v_F\Omega/E_F$, where Ω is the frequency of substrate optical modes, v_F is the Fermi velocity of carriers in graphene, and $E_F = k_BT_z$ is the Fermi energy.[7]

To qualitatively study the impact of gate dielectric thickness on device output characteristics and simplify the analysis, we make the saturation velocity a carrier-density-independent parameter. We first exclude the effect of velocity saturation in the drain current calculation by setting a very large saturation velocity. Furthermore, we assume an ideal gate dielectric with a zero interface trap density ($C_{it} = 0$ μF/cm^2) and zero impurity doping ($V_{dirac} = 0$ V). Figure 2a shows the simulated output characteristics from 500 nm long devices with three different dielectric thicknesses (EOT = 1, 5, 20 nm). The gate voltage is 1 V and source is connected to ground for all simulations. Note that the drain current is normalized to its value at $V_{ds} = 1$ V for all curves. As can be seen in Figure 2a, a thinner EOT delivers an improved saturation behavior, and the minimum g_{ds} approaches to zero for EOT = 1 nm. When V_{ds} increases to 1 V (point a in Figure 2a), the gate to channel voltage at the drain-end becomes 0 V and the Fermi level is at the center of the Dirac cone—no gate

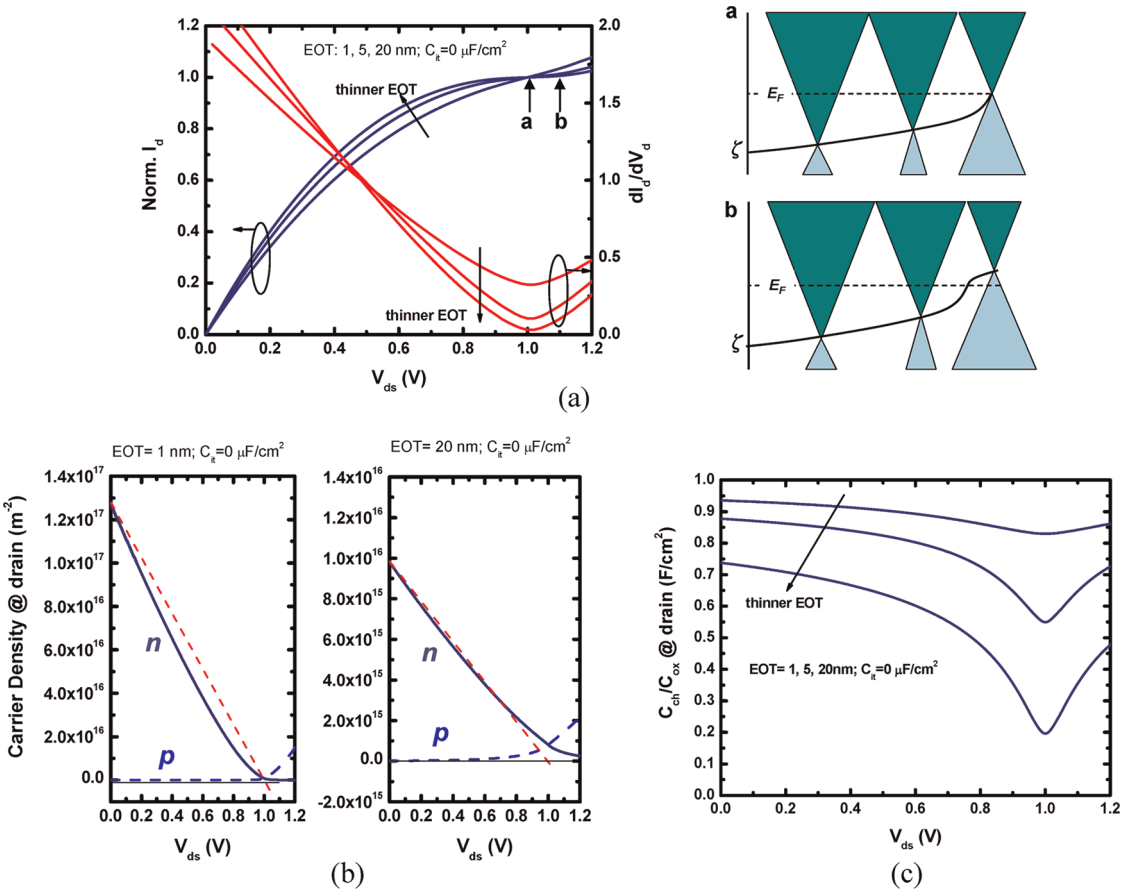

Figure 2. (a) Simulated output characteristics for 500 nm channel device with EOT = 1, 5, 20 nm. C_{it} = 0 μF/cm^2 is assumed. (b) Simulated electron density and hole density at the drain-end for devices with EOT = 1 nm (left) and 20 nm (right). (c) Gate to channel capacitance normalized to C_{ox} as a function of drain−source voltage at the drain-end.

induced carriers at drain. A further increase of V_{ds} moves the charge neutrality point into the channel (point b in Figure 2a), and hole conduction starts to occur at the drain-end while electron conduction still dominates at the source-end.

The improvement of current saturation from thinning the dielectric can be understood by looking at the carrier density as a function of drain bias at the drain-end, which is shown in Figure 2b. Both the electron density and the hole density are plotted, and the dashed line represents the curve with a fixed gate to channel capacitance ($C_{ch} = ((n+p)/(V_g - V_c)) = ((n+p)/(V_g - V_d))$ when $C_{it} = 0$); that is, carrier density is $C_{ch} \cdot V_g$ at 0 V V_d and is 0 at 1 V V_d. There are two distinct features in Figure 2b: (1) n_i is a significant portion of the total carrier density for the device with EOT = 20 nm. Since n_i is not modulated by $V_g - V_d$, it reduces electron depletion as $V_g - V_d$ diminishes and degrades the saturation behavior. On the other hand, due to a stronger gate control in EOT=1 nm, n_i becomes important only at V_{ds} very close to 1 V. (2) Electrons deplete much faster than the fixed C_{ch} line for most V_{ds} in EOT = 1 nm. It is, however, not observed in the curve with EOT = 20 nm. This faster depletion rate leads to a stronger drain current saturation. We attribute the second point above to the strong quantum capacitance limit in the device with small EOT. Figure 2c shows C_{ch}/C_{ox} *vs* V_{ds} where C_{ch} can be calculated by $C_{ch} = (C_{ox}C_q)/(C_{ox} + (C_q + C_{it}))$ from the capacitance network in Figure 1b and it represents the relationship between $V_g - V_d$ and the amount of charge in the channel. When the Dirac point moves toward the device drain-end as V_{ds} approaches to 1 V, graphene's low DOS starts to limit the allowed carrier density induced by $V_g - V_d$, thus it lowers C_{ch}, particularly in the device with larger C_{ox}.

Next, the role of the interface trap is considered. It is inevitable that interface traps exist in the graphene FET. Several recent works indicate that lowering D_{it} is critical for obtaining saturated output characteristics.[10,11] The effect of interface traps on transistor operation is investigated by the similar $C_{ch}/C_{ox} - V_{ds}$ simulations (Figure 3a). It can be seen that interface traps effectively suppress the gate-to-channel control and they show a much greater impact on devices with large EOT. The quantum capacitance effect also gets masked by C_{it} for large EOT. The simulated output characteristics for devices with C_{it} = 0.5 μF/cm^2 and C_{it} = 5 μF/cm^2 are shown in Figure 3b and Figure 3c, respectively. The curve with large EOT exhibits a high

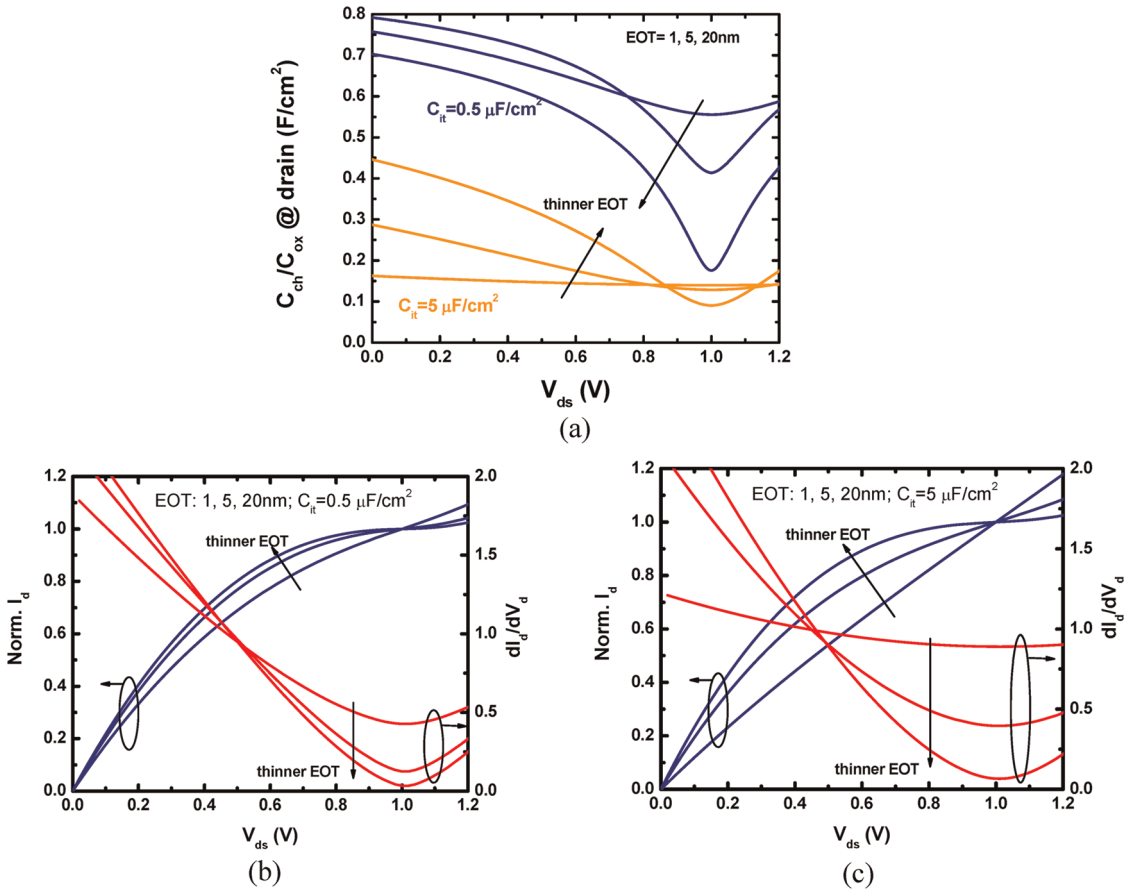

Figure 3. (a) Calculated C_{ch}/C_{ox} as a function of drain-source voltage at the drain-end for devices with nonzero interface traps. (b) Simulated output characteristics for 500 nm channel device with EOT = 1, 5, 20 nm and C_{it} = 0.5 μF/cm^2. (c) Simulated output characteristics with C_{it} = 5 μF/cm^2.

sensitivity to C_{it} and becomes almost linear for C_{it} = 5 μF/cm^2. On the contrary, the curve with 1 nm EOT remains in excellent saturation throughout different C_{it}.

Having explained how thin gate dielectric can improve the drain saturation using the model, we now come back to the data from the embedded gate device. A figure-of-merit for transistors that is of particular importance in analog/RF applications is the intrinsic gain, $G_{in} = g_m/g_{ds}$.[22] The nonsaturating nature of previous graphene FETs yielded high g_m but with similarly high g_{ds}, which resulted in gains rarely greater than unity. The measured g_m, g_{ds}, and G_{in} from the 500 nm long thin dielectric device at V_{gs} = 1.2 V are plotted in Figure 4a. It is evident that these thin EOT graphene FETs can easily achieve $G_{in} > 1$ at a wide range of bias conditions, and yield a high peak gain, which is about 34 for 1.2 V V_{gs}. As a direct result of drain current saturation, Figure 4b shows s-parameter measurement results which indicate that these devices feature AC open-circuit voltage gain (up to 11 dB) and power gain when driving a 50 ohm load impedance (S21 > 1). The successful demonstration of power gain is a critical step for building graphene RF circuits. It is also interesting to note that negative differential resistance (NDR) can be measured in our devices under certain bias conditions. Figure 4c) shows four different devices on the same chip showing NDR. As mentioned earlier, despite the exclusion of the effect of velocity saturation, the model predicts g_{ds} approaches to zero from devices with thin EOT. It is understandable that g_{ds} can become negative once the high field mobility model eq 7 is included, as shown in Figure 4d. NDR becomes more distinct for curves with lower v_{sat}.

CONCLUSION

In summary, a surface-potential-based model for single gate graphene FET in the diffusive transport regime has been derived. Using this model, we found that thinning the gate dielectric can improve the drain current saturation by at least three mechanisms: it reduces the impact from thermally excited carriers, it accelerates the carrier depletion in graphene due to the strong quantum capacitance limit, and it significantly reduces the influence from interface traps. To prove this concept, submicrometer graphene FETs made from large-scale CVD graphene with an

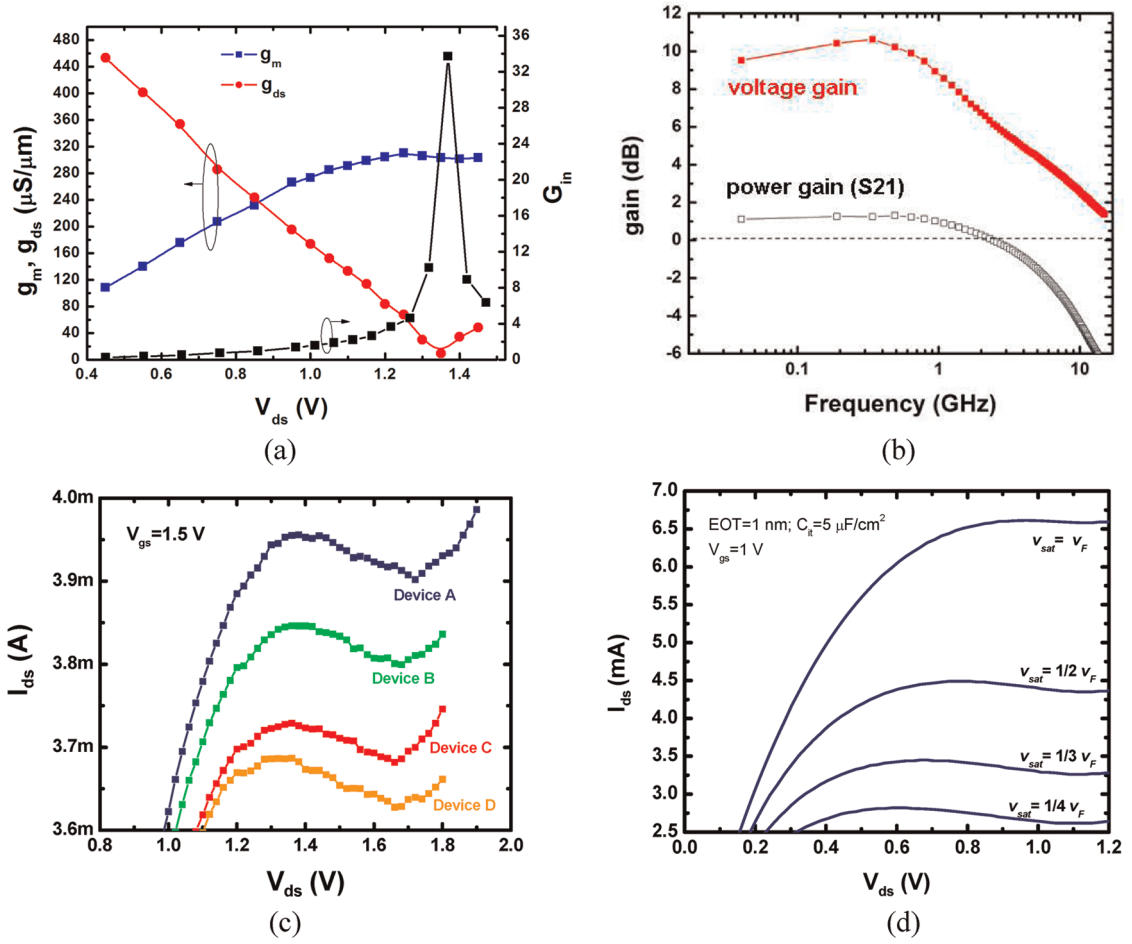

Figure 4. (a) Measured g_m, g_{ds}, and $G_{in} = g_m/g_{ds}$ across a range of drain bias at V_{gs}= 1.2 V. (b) Measured frequency response of extrinsic voltage gain and power gain (S21) from s-parameter measurements. (c) Measured NDR effect from four devices on the same chip. (d) Simulated $I_{ds}-V_{ds}$ with various v_{sat}.

ultrathin gate dielectric have been fabricated. They show clear current saturation, high intrinsic gain, and more importantly, both AC voltage gain and AC power gain. This study provides an important insight into the proper RF device design using graphene.

METHODS

In a 200 mm silicon production fab, beginning with intrinsic Si wafers, 1 μm thick SiO_2 was thermally grown at 1050 °C in a wet oxidation furnace. The wafer was then spin-coated with photoresist and patterned using an ASML Deep UV stepper. High power reactive ion etching with a mixture of CHF_3 and Ar for 15`0 s was used to remove ~200 nm SiO_2, and the photoresist was stripped off in oxygen plasma. Gate material of ~500 nm was deposited. The wafer was then polished in a Westech CMP system. Ion-implantation was performed in an Applied Materials ion implant system using As with an energy of 2 keV and a dose of 1 × 10^{16} ions/cm^2. HfO_2 (44 Å) was then deposited at 500 °C in a TEL CVD system to cover the whole wafer and an HBr-based RIE process was used to etch open the contact pad to the gate. After CVD-grown graphene was transferred, photoresist was again patterned in a DUV system and the exposed graphene area was etched away in a Unaxis RIE system with a 100 W plasma maintained by 30 sccm O_2. Photolithographic patterning was used to define source/drain electrodes and electron beam evaporation was used to sequentially deposit 0.5 nm Ti, 30 nm Pd, and 30 nm Au followed by a lift-off process in ST-22 resist stripper. The graphene FETs were measured in a semiautomated testing tool with a Keithley 236 source measurement unit connecting to the gate and a Keithley 238 high current source measurement unit connecting to the drain. The C–V measurement was done in the same tool with an Agilent E4980A capacitance meter. All measurements were performed at room temperature under N_2 gas flow. S-parameter measurements were carried out up to 30 GHz using a HP8510 vector network analyzer with groundsignal-ground (GSG) coplanar probes.

Conflict of Interest: The authors declare no competing financial interest.

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